A	pplication No.	Applicant(s)	
11	0/824,297	FRANCH ET AL.	
	xaminer	Art Unit	
G	ail Verbitsky	2859	
The MAILING DATE of this communication appears I claims being allowable, PROSECUTION ON THE MERITS IS (Of erewith (or previously mailed), a Notice of Allowance (PTOL-85) or OTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGH the Office or upon petition by the applicant. See 37 CFR 1.313 and	R REMAINS) CLOSED in other appropriate comm ITS. This application is:	n this application. If not included unication will be mailed in due course. TH I	≀ S ativ
This communication is responsive to <u>amendment filed on 04/0</u>	<u>03/2007</u> .	•	
The allowed claim(s) is/are 2 -5,7,9-11,33-36,39-40,44-47,49-	<u>53</u> .		
. ☐ Acknowledgment is made of a claim for foreign priority unde	r 35 U.S.C. § 119(a)-(d)	or (f).	
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3. ☐ Copies of the certified copies of the priority documents have be			e
International Bureau (PCT Rule 17.2(a)).		a aa manana anaga appinaanan nom ma	-
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" of the noted below. Failure to timely comply will result in ABANDONMENTHIS THREE-MONTH PERIOD IS NOT EXTENDABLE. A SUBSTITUTE OATH OR DECLARATION must be submitted.	NT of this application.		*
INFORMAL PATENT APPLICATION (PTO-152) which gives r	reason(s) why the oath o	r declaration is deficient.	
. CORRECTED DRAWINGS (as "replacement sheets") must b			
(a) ☐ including changes required by the Notice of Draftsperson	's Patent Drawing Revie	w (PTO-948) attached	
1) hereto or 2) to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examiner's A Paper No./Mail Date	mendment / Comment o	r in the Office action of	
Identifying indicia such as the application number (see 37 CFR 1.84 each sheet. Replacement sheet(s) should be labeled as such in the	(c)) should be written on t header according to 37 Cl	he drawings in the front (not the back) of FR 1.121(d).	
 DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT FO 	of BIOLOGICAL MAT OR THE DEPOSIT OF BI	ERIAL must be submitted. Note the OLOGICAL MATERIAL.	
Attachment(s)			
Notice of References Cited (PTO-892)	5. Notice of Ir	formal Patent Application	
☐ Notice of Draftperson's Patent Drawing Review (PTO-948)		ummary (PTO-413), /Mail Date	
☐ Information Disclosure Statements (PTO/SB/08),		Amendment/Comment	
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Paper No./Mail Date .	o. 🗀 Examiners		

Application/Control Number: 10/824,297

Art Unit: 2859

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Peterson on April 13, 2007.

The application has been amended as follows:

Claim 52 has been replaced with: An integrated circuit (IC) comprising: a plurality of devices connected together and forming circuits; a switchable current source selectively providing a known current to a PN junction in at least one of said plurality of devices, said switchable current source comprising: a constant current source, and a clamping device selectively shunting current from said constant current source; a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature; wherein said plurality of devices includes a plurality of field effect transistors (FETs) and said PN junction is a FET body to source/ drain junction; and wherein said FET body is P-type silicon body layer in a NFET and said NFET is in a CMOS inverter.

Claim 53 has been replaced with: A CMOS integrated circuit (IC) comprising: a plurality of field effect transistors (FETs) forming CMOS circuits; at least one CMOS circuit comprising: a constant current source, and a clamping device selectively shunting current from said constant current source to a PN junction in one FET in said at least one CMOS circuit; a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature; wherein said PN junction is a FET body to source/drain junction; wherein said CMOS IC is on a silicon on insulator (SOI) IC chip; and wherein said FET body is P-type silicon body layer in a NFET and said NFET is in a CMOS inverter.

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the PTO-892 and not mentioned above disclose related devices and methods.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gail Verbitsky whose telephone number is 571/272-2253. The examiner can normally be reached on 7:30 to 4:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571/272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GKV

Gail Verbitsky

Primary Patent Examiner, TC 2800

Melesku

April 13, 2007